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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,160	01/29/2007	Kenji Kohiro	3885-0109PUS1	9498

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
07/14/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/560,160	KOHIRO ET AL.	
	Examiner	Art Unit	
	ORI NADAV	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-18* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102/3

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Inoue et al. (5,019,874) in view Mochizuki et al. (6,696,711).

Regarding claim 18, Inoue et al. teach in figure 5 and related text a method of producing a compound semiconductor, which comprises

forming on a GaAs substrate 22 an InP crystal or a compound semiconductor crystal, wherein the compound semiconductor crystal has a lattice constant is closer to that of InP than that of GaAs (InP 25 or 23b),

wherein the InP crystal or the compound semiconductor crystal is formed on the GaAs substrate via an InGaP buffer layer or an InGaAsP buffer layer 24 and

the thickness of InGaP buffer layer or an InGaAsP buffer layer 24 is not less than 5 nm and not greater than 300 nm.

Regarding the claimed limitation of a GaAs substrate, since Inoue et al.'s structure is formed on layer 22, and layer 22 supports Inoue et al.'s structure, then layer 22 can be considered as at least part of the base (substrate) of the structure.

In the alternative, Inoue et al. teach that it is advantageous to use a GaAs substrate (column 1, lines 15-23).

Mochizuki et al. in figure 2 and related text using a GaAs substrate 1.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a GaAs substrate in Inoue et al.'s structure in order to simplify the processing steps of making the device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al. (6,696,711) in view of Inoue et al. (5,019,874).

Regarding claim 18, Mochizuki et al. teach in figure 2 and related text a method of producing a compound semiconductor, which comprises

forming on a GaAs substrate 1 an InP crystal or a compound semiconductor crystal, wherein the compound semiconductor crystal has a lattice constant is closer to that of InP than that of GaAs (3, 4 or 6),

wherein the InP crystal or the compound semiconductor crystal is formed on the GaAs substrate via an InGaP buffer layer or an InGaAsP buffer layer 2.
Mochizuki et al. do not teach that the thickness of InGaP buffer layer or an InGaAsP buffer layer 2 is not less than 5 nm and not greater than 300 nm.
Inoue et al. teach in figure 5 and related text that the thickness of InGaP buffer layer or an InGaAsP buffer layer 24 is not less than 5 nm and not greater than 300 nm.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a thickness of InGaP buffer layer or an InGaAsP buffer layer not less than 5 nm and not greater than 300 nm, in Mochizuki et al.'s structure in order to reduce the size of the device and in order to improve the device characteristics.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over (Mochizuki et al. and Inoue et al.) or over (Inoue et al. and Mochizuki et al.), as applied to claim 18 above, and further in view of Ohkubo et al. (5,492,860).
Regarding claim 9, (Mochizuki et al. and Inoue et al.) and (Inoue et al. and Mochizuki et al.) teach substantially the entire claimed structure, as applied to claim 18 above, except stating that the growth of the InGaP buffer layer or the InGaAsP buffer layer is conducted at a temperature of not lower than 400 ℃ and not higher than 600 ℃, and the growth of the InP crystal or a compound semiconductor crystal whose lattice

constant is closer to that of InP than that of GaAs is conducted at a temperature of not lower than 400 ℃ and not higher than 700 ℃ .

Ohkubo et al. teach that the growth of the InGaP buffer layer or the InGaAsP buffer layer is conducted at a temperature of not lower than 400 ℃ and not higher than 600 ℃, and the growth of the InP crystal or a compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs is conducted at a temperature of not lower than 400 ℃ and not higher than 700 ℃ .

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to grow the InGaP buffer layer or the InGaAsP buffer layer at a temperature of not lower than 400 ℃ and not higher than 600 ℃, and to grow the InP crystal or a compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs is conducted at a temperature of not lower than 400 ℃ and not higher than 700 ℃ , in Mochizuki et al.'s structure in order to improve the device characteristics and the crystal quality of the layers by obtaining the required thickness of the layers.

Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mochizuki et al. in view of Ohkubo et al. (5,492,860).

Regarding claim 10, Mochizuki et al. teach in figure 2 and related text a method of producing a compound semiconductor by growing on a GaAs substrate InP crystal or a compound semiconductor crystal whose lattice constant is closer to that of InP than that

of GaAs, which method of producing the compound semiconductor is characterized in that:

an InGaP buffer layer or an InGaAsP buffer layer 2 is grown on the GaAs substrate 1; and

the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs (3 or 4) is grown on the InGaP buffer layer or the InGaAsP buffer layer;

wherein an InP buffer layer 6 is grown on the InGaP buffer layer or the InGaAsP buffer layer.

Mochizuki et al. do not explicitly state that the InP buffer layer is raised in temperature to a prescribed annealing temperature and annealed, and the temperature is lowered to a prescribed crystal growth temperature for growing the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, whereafter the InP crystal or the compound semiconductor crystal is grown.

Ohkubo et al. teach an InP buffer layer is raised in temperature to a prescribed temperature, and the temperature is lowered to a prescribed crystal growth temperature for growing the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, whereafter the InP crystal or the compound semiconductor crystal is grown.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the InP buffer layer by raising the temperature to a prescribed annealing temperature and annealed, and the temperature is lowered to a

prescribed crystal growth temperature for growing the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, in prior art's device, in order to improve the crystal quality of the layers.

Regarding claims 11 and 13, Ohkubo et al. teach that the growth of the InGaP buffer layer or the InGaAsP buffer layer is conducted at a temperature of not lower than 400 ℃ and not higher than 600 ℃ and the growth temperature of an InP buffer layer is not lower than 400 ℃ and not higher than 550 ℃. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to grow the InGaP buffer layer or the InGaAsP buffer layer at a temperature of not lower than 400 ℃ and not higher than 600 ℃ and the growth temperature of an InP buffer layer is not lower than 400 ℃ and not higher than 550 ℃, in Mochizuki et al.'s structure in order to improve the device characteristics and the crystal quality of the layers by obtaining the required thickness of the layers.

Regarding claim 12, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the InP buffer layer to a thickness of not less than 20 nm and not greater than 200 nm, in prior art's device in order to reduce the size of the device.

Regarding claim 14, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's device by forming the InP buffer

layer in temperature to a prescribed annealing temperature and annealed, and then, before growing the InP crystal or compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, an operation for lowering the temperature from the prescribed annealing temperature to a prescribed crystal growth temperature and again raising it to the prescribed annealing temperature is repeated not less than one time and not more than five times, whereafter the temperature is lowered to the prescribed crystal growth temperature, in order to improve the crystal quality of the layers.

Regarding claims 15 and 16, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's device by using the prescribed annealing temperature not lower than 650 (or 400) ℃ and not higher than 730 (or 700) ℃ in order to have better control over the growth of the layers.

Regarding claim 17, the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs is InGaAs or InAlAs crystal in prior art's device.

Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. and Mochizuki et al., as applied to claim 18 above, and further in view of Ohkubo et al. (5,492,860).

Regarding claim 10, Inoue et al. and Mochizuki et al. teach substantially the entire claimed structure, as applied to claim 18 above, including an InP buffer layer 23b (Inoue et al., figure 5) is grown on the InGaP buffer layer or the InGaAsP buffer layer. Inoue et al. and Mochizuki et al. do not explicitly state that the InP buffer layer is raised in temperature to a prescribed annealing temperature and annealed, and the temperature is lowered to a prescribed crystal growth temperature for growing the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, whereafter the InP crystal or the compound semiconductor crystal is grown.

Ohkubo et al. teach an InP buffer layer is raised in temperature to a prescribed temperature, and the temperature is lowered to a prescribed crystal growth temperature for growing the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, whereafter the InP crystal or the compound semiconductor crystal is grown.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the InP buffer layer by raising the temperature to a prescribed annealing temperature and annealed, and the temperature is lowered to a prescribed crystal growth temperature for growing the InP crystal or the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, in prior art's device, in order to improve the crystal quality of the layers.

Regarding claims 11 and 13, Ohkubo et al. teach that the growth of the InGaP buffer layer or the InGaAsP buffer layer is conducted at a temperature of not lower than 400 °C and not higher than 600 °C and the growth temperature of an InP buffer layer is not lower than 400 °C and not higher than 550 °C. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to grow the InGaP buffer layer or the InGaAsP buffer layer at a temperature of not lower than 400 °C and not higher than 600 °C and the growth temperature of an InP buffer layer is not lower than 400 °C and not higher than 550 °C, in prior art's structure in order to improve the device characteristics and the crystal quality of the layers by obtaining the required thickness of the layers.

Regarding claim 12, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the InP buffer layer to a thickness of not less than 20 nm and not greater than 200 nm, in prior art's device in order to reduce the size of the device.

Regarding claim 14, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's device by forming the InP buffer layer in temperature to a prescribed annealing temperature and annealed, and then, before growing the InP crystal or compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs, an operation for lowering the temperature from the prescribed annealing temperature to a prescribed crystal growth

temperature and again raising it to the prescribed annealing temperature is repeated not less than one time and not more than five times, whereafter the temperature is lowered to the prescribed crystal growth temperature, in order to improve the crystal quality of the layers.

Regarding claims 15 and 16, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form prior art's device by using the prescribed annealing temperature not lower than 650 (or 400) ℃ and not higher than 730 (or 700) ℃ in order to have better control over the growth of the layers.

Regarding claim 17, the compound semiconductor crystal whose lattice constant is closer to that of InP than that of GaAs is InGaAs or InAlAs crystal in prior art's device.

Response to Arguments

Applicant's arguments with respect to claims 9-18 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ORI NADAV whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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